METHOD AND APPARATUS FOR IMPROVING IMAGES PROVIDED BY SPATIAL LIGHT MODULATED (SLM) DISPLAY SYSTEMS

Cross Reference to Related Applications

[0001] This application claims benefit of United States provisional patent application serial number 60/555,253, filed Mar. 22, 2004, which is herein incorporated by reference.

Field of the Invention

The present invention generally relates to Spatial Light Modulation (SLM) display systems, and in particular to filters and filter methods for use in SLM systems.

Background of the Invention

[0002] Spatial Light Modulating (SLM) systems include Digital Light Processing ™ (DLP™) systems. DMD and DLP ™ are trademarks of Texas Instruments Corporation. Recent developments in SLM technology rely on SLM elements that provide diamond shaped shaped pixels instead of square shaped pixels. Processing techniques for SLM systems include a so called "smooth pixel" processing technique. According to the smooth pixel technique, a displayed image is formed by combining a first set of pixels with a second set of pixels. The second set is displaced from the first set. The combined first and second pixel sets form a displayed image.

[0003] In one example SLM system, an SLM arra;y comprising a number of SLM elements provides first and second pixel sets for each incoming picture, or frame, to be displayed. The combined pixels from the first and second pixel sets provide more displayed pixels than the number of SLM elements employed to provide the pixel sets.

[0004] However, a drawback is associated with this technique. Pixels of the first and second pixel sets overlap in the displayed image. At least some of the pixels from the first set effectively overlap at least some of the pixels from the second set. As a result, when the pixel sets are displayed together so as to form an image, light in the regions of overlapping pixels is a combination of light from each of the

overlapping pixels. This sometimes results in brighter than intended, or less bright than intended image portions.

[0005] Thus, some loss of image quality is incurred with this technique as compared to other display techniques. Accordingly, image processing devices and methods are needed that account for distortion due to overlapping pixels in displayed pixel sets of SLM devices.

Summary of the Invention

According to various embodiments of the invention methods and systems for reducing distortion in images provided by display systems(100) employing Spatial Light Modulating (SLM) elements are provided. A method according to one embodiment of the invention comprises steps of providing a set (620) of pixel values corresponding to pixels of an image to be displayed. The number of pixel values comprising the set is greater than the number of available SLM elements. At least some of the pixel values are adjusted to provide a set of adjusted pixel values (678). At least a first set of pixels and a second set of pixels are generated from the set of adjusted pixel values. The image is displayed as a matrix of pixels (450) comprising the first set of pixels (410) and the second set of pixels (430). At least one of the pixels of the first set overlaps at least one of the pixels of the second set and the adjusting step is carried out by adjusting pixel values of the set of pixel values to compensate for image distortion due to overlapping pixels of the matrix.

Brief Description of the Drawings

[0006] Embodiments of the present invention will be described below in more detail, with reference to the accompanying drawings, in which:

[0007] Fig. 1 is a block diagram illustrating a display system including an array of spatial light modulation (SLM) elements suitable for implementing various embodiments of the invention.

[0008] Fig. 2 is a block diagram illustrating in more detail the electronics subsystem of the display system illustrated in Fig. 1.

[0009] Fig. 3 is a block diagram illustrating an SLM system including a pixel filter according to an embodiment of the invention.

[0010] Fig. 4 is a diagram illustrating relationship between received pixel data, adjusted pixel data and a pixel matrix according to an embodiment of the invention.

[0011] Fig. 5 is a block diagram of a pixel filter according to an embodiment of the invention.

[0012] Fig. 6 illustrates an example lookup table suitable for use in the pixel data filter of Fig. 5 according to an embodiment of the invention.

[0013] Fig. 7 is a detailed diagram of an embodiment of the pixel data processing device illustrated in Fig. 5.

Detailed Description

[0014] Spatial Light Modulator (SLM) devices find increasing use in a wide range of imaging applications such as video image projection and printing. Typical spatial light modulators include devices such as Liquid Crystal Devices (LCDs) and digital micro-mirror devices (DMDs^{tm}). A typical spatial light modulator comprises a two-dimensional array of modulator elements that operate upon incident light in order to form a two-dimensional image on a display surface. LCD based devices use light polarization characteristics in order to modulate each light element in the array. DMD ™ based devices use an array of tiny micro-mirrors to modulate individual light elements. Each element in a spatial light modulator array exhibits a variable light intensity in response to a corresponding drive voltage level. In one embodiment of the invention, each element in an SLM array corresponds to at least one pixel of a displayed image.

Fig. 1 is a pictorial diagram illustrating an example system 100 including a Spatial Light Modulating (SLM) array 500 suitable for implementing various embodiments of the present invention. System 100 comprises at least one light source 301 coupled to an optical system 400. Optical system 400 comprises relay and illumination optics 300 and projection optics 200. Optical system 400 includes at least one array 500 of spatial light modulating elements 502. According to an embodiment of the invention array 500 comprises a semiconductor-based array of reflective light elements 502. According to one embodiment of the invention, SLM array 500 comprises a binary Pulse Width Modulated (PWM) array 500 of light switching elements 502. In one embodiment, elements 502 of PWM array 500 comprise micro-electromechanical system (MEMS) devices, for example, mirrors of a Digital Micromirror Device ^{tm} (DMD)^{tm}.

An electronics subsystem 600 includes an input for receiving a video signal 601 and an output coupled to the SLM array 500. Electronics subsystem 600 processes incoming video signal 601 so as to provide PWM signals to drive elements 502 of array 500. The PWM signals control the angle and dwell time of elements 502 of array 500 in accordance with pixel values provided by video signal 601. Properties, for example, brightness, of pixels displayed on display screen 499 are related to the dwell time of respective corresponding micro-mirror elements 502.

Electronics subsystem 600 receives a video signal 601 from a source of video signals (not shown). Video signal 601 comprises video image data corresponding to video images to be projected and displayed on display device 499. Electronics subsystem 600 processes video signal 601 and provides a processed video signal 602 to drive array 500.

Optics system 400 comprises at least one relay and illumination optics portion 300, at least one projection optics portion 200 and at least one light source 301. Light from light source 301 is transmitted through at least one relay optics portion 300. Light from relay optics portion 300 is projected onto light reflecting elements 502 of SLM array 500.

According to embodiments of the invention, video signal 601 is provided by at least one of a wide variety of suitable video signal sources. Suitable video signal sources include for various embodiments of the invention are too numerous to recite in total. However, some examples include, but are not limited to, digital versatile disk (DVD) systems, set top boxes, broadcast video sources, Internet video sources, cable video sources, satellite video sources, wireless and telephonic sources, to name but a few. Embodiments of the invention comprise digital video intermediate systems wherein video sources include film, telecines, video masters and the like.

[0015] Regardless of video signal source, suitable video signals 601 for embodiments of the invention include, among others, analog video signals, digital video signals, component video signals and composite video signals. Suitable signal formats include, among others, National Television Standards Committee (NTSC) format, Phase Alternate Lines (PAL) format, and PAL plus format. Any video format providing pixel values corresponding to pixels of an image to be displayed is suitable for use in various embodiments of the invention.

[0016] Figure 2 illustrates functional blocks of the electronics subsystem 600 illustrated in Fig. 1 acccording to an embodiment of the invention. Electronics subsystem 600 comprises a receiver 610 for receiving video signal 601. Receiver 610 is coupled to video processing unit 640. Video processing unit 640 is coupled to SLM array driver 690.

[0017] According to embodiments of the invention, receiver 610 receives video signal 601 at an input. In an example embodiment of the invention, receiver 610 decodes video signal 601 and performs Analog to Digital (A/D) conversion, Luminance-chrominance separation (Y/C separation), and chrominance demodulation of video signal 601 in accordance with conventional video signal receiving and decoding techniques,

[0018] According to embodiments of the invention, video processing unit 640 further provides video processing functions, for example, progressive scan conversion, and resampling of video signal 601 in accordance with conventional techniques. Video processing unit 640 is coupled to an SLM device driver 690. SLM device driver 690 provides drive signals for driving elements 503 of SLM array 500. According to an embodiment of the invention, video processor provides enhanced Chrominance (2C) and Luminance (2Y) signals for use by driver 690 in driving elements 503 of array 500 so as to modulate light in accordance with video signal 601.

[0019] Video processing unit 640 includes pixel filter 320 coupled to a pixel group generator 680. In one embodiment of the invention, pixel group generator 680 is a conventional device providing pixel groups for so called, "smooth pixel" processing techniques. According to one embodiment of the invention, pixel filter 320 is implemented by programming a processor of video processing unit 640 so as to implement pixel processing functions in accordance with the various embodiments of the invention described herein. In alternative embodiments of the invention, functions of pixel filter 320 are provided by hardware without the need for programming a processor. Still other embodiments of the invention implement some functions of pixel filter 320 in hardware while other functions are implemented by a processor programmed for carrying out the other functions. However, as those of ordinary skill in the art will readily appreciate upon reading the specification herein, a wide variety of hardware and software combinations will be suitable for implementing the invention. Therefore, the pixel filter of the invention is not limited to one specific hardware and processor arrangement.

[0020] According to one embodiment of the invention, receiver portion 610 provides luminance (Y) signals 620 to pixel filter 320 based upon video signal 601.

According to one embodiment of the invention, receiver portion 610 provides chrominance (C) signals 649 to pixel filter 320 based upon video signal 601.

[0021] In some embodiments of the invention, video signal processor 640 provides further processing functions including, for example, color space conversion, gamma correction removal, error diffusion, on screen display capability, Red, Green, Blue (RGB) input receiving capability, and user operable image controls. In one embodiment of the invention, driver 690 includes a Field Programmable Gate Array (FPGA).

[0022] In one embodiment of the invention Field Programmable Gate Array (FPGA) 690 receives RGB video signals from video signal processor 640 and provides PWM control functions, image reformatting, bit plane conversion and DMD drive signal functions based, at least in part, on the RGB video signals. According to embodiments of the invention, system 600 further comprises memory 622 and timing and control circuits 621 for electronics subsystem 600.

[0023] As will be readily appreciated by those of ordinary skill in the art processors are commonly embedded throughout systems in a wide variety of configurations and capabilities. Any processor configuration implementing the inventive circuits, systems and methods described herein remain within the scope of the invention.

[0024] Fig. 3 is a block diagram illustrating an embodiment of the invention. Display screen 499 is arranged with respect to SLM array 500 so as to display an image comprising a matrix 450 of pixels. Matrix 450 comprises at least a first pixel group 410 and a second pixel group 430. (also illustrated in Fig. 4). According to alternative embodiments of the invention, matrix 450 comprises more than two pixel groups. According to an embodiment of the invention, the number of pixels comprising matrix 450 is greater than the number of elements 502 of SLM array 500 used to provide first and second pixel groups 410 and 430.

[0025] As illustrated in Fig. 3, light from a light source 301 is transmitted through relay optics subsystem 300. In one embodiment of the invention, optics subsystem 300 includes a means for providing colored light. According to one embodiment of the invention, optics subsystem 300 includes a color wheel alternately producing red, green and blue light. According to an alternative embodiment of the invention, light source 301 comprises a red light source, a green light source and a blue light source.

The colored light is projected onto array 500 and reflected from array 500. Light reflected from array 500 is provided to display 499 via projection optics subsystem 200.

[0026] Elements 502 of array 500 are driven in accordance with pixel values provided by pixel data set 620. Each pixel of matrix 450 corresponds to a pixel value of incoming pixel data set 620. Pixel data set 620 is generated based upon video signal 601. In Fig. 3 pixel data set 620 is represented by an arrangement of letters A through O.

[0027] Pixel processor 320 adjusts pixel values of pixel data set 620 and provides adjusted pixel data set 678 to pixel group generator 675. In Fig. 3 adjusted pixel data set 678 is represented by an arrangement of letters A' through O'. Pixel group generator 675 separates adjusted pixel data set 678 into first and second pixel data groups (679 and 680). In one embodiment of the invention, pixel group generator 675 operates in accordance with a known pixel processing technique such as a "smooth pixel' processing technique. According to smooth pixel processing, an input pixel data set, for example, 620 is separated into first and second pixel data groups . The first and second pixel data groups provide first and second pixel groups comprising a displayed matrix .

[0028] However, conventional pixel processing techniques do not include pixel filter 320, nor do conventional systems provide an adjusted pixel data set 678 to a pixel generator 675. Accordingly, first and second pixel groups 410 and 430 comprising matrix 450 according to the invention provide significant advantages over conventional smooth pixel processing techniques.

[0029] Fig. 4 illustrates the relationship between pixel data set 620, adjusted pixel data set 678, pixel data groups 679 and 680, pixel groups 410 and 430, and pixel matrix 450 according to an embodiment of the invention. As illustrated in Fig. 4, first pixel group 410 comprises rows h and columns c of adjacent pixels 412. For convenience, a single indicator 412 indicates individual pixels of group 410 . Second pixel group 430 comprises rows *h* and columns *c* of adjacent individual pixels 432.

[0030] Pixel groups 410 and 430 are projected onto display screen 499 so as to appear displaced from each other, for example, by a distance *d*. In one embodiment of the invention, pixel groups 410 and 430 are displaced from each other in a direction substantially in x-direction of the plane of the surface of display screen 499.

[0031] In one example embodiment of the invention, second pixel group 430 is displayed spaced from first pixel group 410 by a distance equal to about half of the height of a single pixel. The resulting pixel matrix 450 therefore comprises overlapping pixels. In other words, individual pixels from first pixel group 410, overlap individual pixels from second pixel group 430.

[0032] In one embodiment of the invention, SLM elements 502 comprise diamond shaped elements. Therefore, pixels of matrix 450 comprise substantially diamond shaped pixels (example illustrated in Fig. 4). However, other pixel shapes, e.g. square pixels, are known, and are suitable for some applications of the invention.

[0033] Fig. 3 illustrates an optical element 210 as one example of conventional means for providing the spacing for pixel groups 410 and 430. Optical element 210 reflects one of pixel sets 410 and 430 onto screen 499 at a first angle $\varnothing_1$. Optical element 210 subsequently projects the other pixel set at a second angle $\varnothing_2$. This technique has the advantage of providing a matrix 450 with more displayed pixels than the number of available elements 502 on SLM device 500. In one embodiment of the invention, the number of pixels comprising matrix 450 is about twice the number of available micro-mirrors 502 of SLM device 500.

[0034] However, the technique described above results in overlapping pixels. Light from each of the overlapping pixels combines. Therefore, the displayed brightness for a given pixel sometimes fails to correspond to the brightness value provided in pixel data set 620. In some cases the displayed brightness of overlapping pixels is greater than the intended brightness. In other cases, the displayed brightness of overlapping pixels is less than the intended brightness.

[0035] According to an embodiment of the invention pixel data set 620 is provided to pixel filter 320. Filter 320 provides modified pixel data set 678. Pixel data groups 679 and 680 are formed from modified pixel data set 678. The pixel values of pixels of pixel data groups 679 and 680 are used to generate pixel groups 410 and 430 respectively. Displayed combined pixel groups 410 and 430 comprise matrix 450.

[0036] In accordance with an embodiment of the invention, pixel filter 320 provides adjusted example data set 678 as represented by the following diagram:

A' B' C' D' E'
F' G' H' I' J'

K' L' M' N' O'

[0037] First pixel data group 679 comprises pixel data labeled A', C', E', G', I', K', M', O. Second pixel data group 680 comprises pixels labeled B', D', F', H', J', 'L, N'. Pixel groups 410 and 430 are generated based on pixel data groups 679 and 680 respectively. Matrix 410 comprises first pixel group 410 and second pixel group 430.

[0038] As can be seen from the drawing of matrix 450, pixels from the first pixel group 410 at least partially overlap pixels of pixel group 430 and vice versa. For example, the G pixel position in the first pixel group 410 is overlapped by the B, F. L and H pixel positions from the second pixel group 430. This overlap causes intensity distortion of the image represented by matrix 410.

[0039] According to an embodiment of the invention, distortion in pixel intensity caused by the overlap is reduced by an image enhancing filter arrangements 320 illustrated in Figs. 3, 5 and 7.

[0040] Figure 5 illustrates an embodiment ofa pixel filter 320 according to an embodiment of the invention. Pixel filter 320 comprises at least one two-dimensional filter that operates on respective pixels of pixel data set 620 in accordance with an array *h* given by:

$$\begin{matrix} & -\alpha & \\ -\alpha & \beta & -\alpha \\ & -\alpha & \end{matrix}$$

wherein β is a scaling factor associated with a pixel of pixel data set 620 from which the intensity distortion is to be removed; and

α is a scaling factor for pixels overlapping the pixel of pixel data set 620 from which the intensity distortion is to be removed.

More particularly, filter 320 adjusts intensity values I of respective pixels of data set 620 by an amount sufficient to compensate for the intensity contribution of pixels overlapping a respective pixel in matrix 450. For example, in Fig. 4, the intensity (I_G) of pixel G in pixel data set 620 is scaled by an amount (β) such that the intensity distortion caused by overlapping pixels B (I_B), F (I_F), L (I_L)and H (I_H)in displayed matrix 450 is reduced. In an

embodiment of the present invention, adjusted pixel G' has an adjusted intensity value $I_{G'}$ in accordance with the relationship illustrated below:

$$I_{G'} = \beta(I_G) - \alpha(I_H + I_L + I_B + I_F) \qquad (1)$$

Wherein:

β is a scaling factor associated with the pixel G from which the intensity distortion is to be removed; and

α is a scaling factor associated with overlapping pixels that are contributing to the intensity of pixel G.

[0041] According to one embodiment of the invention, a relationship between β and α is given by: $\beta = 1 + 4\alpha$. This relationship provides unity DC gain. However, the invention is not limited in this regard. In one embodiment of the invention, α is approximately +1/8 and β is approximately 3/2. Selecting these example scaling factors has been found to provide unity DC gain while compensating for distortion in some embodiments of the invention.

[0042] According to the example above, the pixel data for the example data set 620, and the adjusted data set 678 is represented as follows:

A	B	C	D	E		A'	B'	C'	D'	E'
F	G	H	I	J	→	F'	G'	H'	I'	J'
K	L	M	N	O		K'	L'	M'	N'	O'

[0043] Fig. 5 is a block diagram illustrating an example filter arrangement 320 representing one of three like filters 320a, 320b, 320c illustrated in Fig. 3. Filter 320 implements the relationship described in equation 1 above for each pixel in respective red, green and blue components of component video signal 620. For convenience, the operation of one filter 320 will be described in relation to an example pixel G. Overlapping pixel groups 410 and 430 as shown in Fig. 4. are referred to herein as an example for purposes of discussion. However, it will be understood that each of the pixels comprising incoming pixel set 620 are suitable for processing in the same way to remove intensity distortion caused by overlapping pixels.

[0044] Referring to Fig. 5, a pixel filter 320 according to an embodiment of the invention is illustrated. Pixel filter 320 comprises a delay circuit 646. Delay circuit 646 receives pixel data of pixel data set 620. Delay circuit 646 delays the received pixel data so as to provide pixel data for a plurality of pixels substantially simultaneously. In the example illustrated in Fig. 5, delay circuit 646 provides pixel data for pixels H, L, F and B (overlapping example pixel G in matrix 450.) to adder 648. At the same time, delay circuit 646 provides data for example pixel G to a second scaler 652. Adder 648 provides an output representative of the sum of pixel values for pixels H, L, F and B to a first scaler 651. First scaler 651 applies a scaling factor α to its input to provide a scaled output. Second scaler 652 applies a scaling factor β to its input.to provide a scaled output. The scaled outputs of scalers 651 and 652 are combined by subtractor 653. The difference output of subtractor 653 represents an adjusted value G' for example pixel G. According to one embodiment of the invention, the difference output of subtractor 653 is optionally provided to a limiter. In that case, successive output values provided by limiter 654 comprise adjusted pixel data set 678.

[0045] According to one embodiment of the invention, a scaling factor for first scaler 655 is adjustable by an adjustment factor .X provided by first adjuster, 655. According to one embodiment of the invention, a scaling factor for the second scaler 652 is adjustable by an adjustment factor Y provided by second adjuster 657.

[0046] Figure 6 illustrates a pixel filter control circuit 700 for implementing an embodiment of pixel filter 320 including adjustable scaling factors. Filter control circuit 700 comprises a look up table 150. Look up table 150 stores a plurality of selectable XY pairs of adjustment factors for X 154 and Y 156. Each XY pair of the table corresponds to one of the filter control setting 152 of table 150. In the example illustrated in Fig. 6, eight possible filter control settings, e.g, 0 through 8 are provided. To select scaler adjustment factors X amd Y a filter control signal representing one of the eight control settings is provided at filter control input 688 of table 150, The XY value pair corresponding to the filter control setting selected by input 688 provides adjsustment factors X and Y to first and second adjusters 655 and 657. In that manner, lookup table 150 provides adjustable scaling factors for scalers 655 and 652.

[0047] In one embodiment of the invention, the X and Y values of table 150 maintain a given relationship between scaling factors α and β while permitting adjustment of scaling factors α and β. In one embodiment of the invention, the given relationship between α and β is a unity gain relationship given by:

$$\beta = 1 + \alpha.$$

[0048] Figure 7 is a more detailed diagram of one embodiment of the filter illustrated in Fig. 6. A video signal representing pixel data set 620 is provided to full line delay registers 803 and 805. Line delay registers 803 and 805 delay the video signal by an entire line of displayed video according to one embodiment of the invention. For the purpose of the present example, the delays of line delay registers 803 and 805 are chosen according to the principles illustrated by the following example. When the data for pixel M, for example, is presented at input 620, the output of line delay register 805 will be H and the output of line delay register 803 will be C. As illustrated in Fig. 7, the output of line delay registers 805, 803 and the original video input signal, e.g., M are coupled respectively to a second bank of delay registers 807, 809, and 800. The outputs of delay registers 803 and 800 are added by adder 812. The output of adder 812 is provided to a first input of adder 823.

[0049] A second input to adder 823 is provided as follows. An output of delay element 809 is provided to delay element 811. The output of delay element 811 is provided to one input of adder 813. The other input to adder 813 is provided by the output of delay element 807. A sum output of adder 813 is coupled to the second input to adder 823.

[0050] According to the example above, the sum H+L+B+F. is provided. Pixels H, L, B and F are pixels overlapping pixel G in matrix 450 of Fig. 1. This sum represents a sum of pixel intensity values for each of the pixels that overlap pixel G. The sum H+L+B+F is then scaled by a scaling factor α. Scaling is accomplished in one embodiment of the invention as follows. The sum H+L+B+F is provided to multiplier 814. Multiplier 814 multiplies the sum H+L+B+F accordance with a first multiplier X, indicated at multiplier input 655. The output of multiplier 655 is provided

to divider 651. In the embodiment illustrated In Fig. 7 divider 651 divides the output or multiplier 655 by 32. Therefore, the sum (H + L + B + H) output from adder 823 is scaled by a factor of $x/32$, where 32 is a constant and x/32 comprises scaling factor α. For example if $x = 4$ in Fig. 7, then $\alpha = 4/32$ or 1/8. Accordingly, the scaled sum for pixels in the example above is (1/8)(H+L+B+F).

[0051] Similarly, a second scaling factor β is applied to pixel data value G by providing data value G to multiplier 804. The output of multiplier 804 is provided to a 1/8 divider 652. Therefore, G is scaled by a factor of y/8 comprising scaling factor β. A subtractor 817 provides an output representing the difference between the scaled pixel intensity data value β (G) and the scaled sum of the intensity values of overlapping pixels, i.e., (α)(H+L+B+F)..

[0052] In one embodiment of the invention the output of subtractor 817 is provided to a limiter 654. Limiter 654 maintains the difference value provided by subtractor 817 within a range of pixel intensity values. According to one embodiment of the invention, various additional delay registers, e.g., 819 are provided in the filter circuit in Fig. 7 to allow for circuit settling times.

[0053] It will be appreciated by those of ordinary skill in the art that various other relationships between β and α, e.g., other than unity gain relationships, are possible. Table 600 is suitable for implementing a wide variety of relationships. The other relationships can readily be accomplished by substituting appropriate values of x y pairs in table 600. Advantageously the pairs are customizable such that a specific relationship is maintained between β and α for all values of x and y pairs on the table.

[0054] According to one embodiment of the invention, look up table 150 is implemented in a memory (not shown), for example, a semiconductor memory. In that case, the memory stores values of x and y. The memory includes x and y outputs coupled to inputs x (indicated at 655) and y (indicated at 657) respectively of filter 645 of Fig. 7. In a look up table embodiment comprising eight x,y pairs, x is selectable such that α ranges in 1/32 increments between 0 to 7/32. For the same table, y is selectable such that β ranges from 1 to 15/8 in increments of 1/8.

[0055] Those skilled in the art will readily appreciate that the foregoing filters are capable of implementation in various combinations of software, hardware and/or

firmware. According to one embodiment of the invention, look up table values are stored in an electronic memory. For example, data sets can be stored in a bus register, RAM or other data storage device associated with a DLP system microprocessor. Still, the invention is not limited in regard to memory types, and other suitable methods exist for storing such values. In one embodiment of the invention, filter control values are selectable by a user via a user operable interface with a DLP display system. According to another embodiment of the invention, filter control values are automatically adjusted by a system microprocessor (not shown) provided for controlling the DLP system.

[0056] Further, while Figs. 5 and 7 represent embodiments of filters according to the invention, those skilled in the art will recognize that the invention is not limited to particular component arrangements. For example, other filter architectures are possible for implementing the invention. That is, other filter architectures are suitable for operating on pixel values so as to adjust pixel intensity to at least partially compensate for the intensity distortion caused by overlapping pixelsl. Further, while it is be advantageous in many embodiments of the invention to select $\beta = 1 + 4\alpha$, the invention is not limited in this regard to such values. The values of β and α are selectable to have other values and relationships according to various embodiments of the invention.